2.(Amended) The [transistor] system of claim 1[, wherein the gate comprises polycrystalline silicon carbide] wherein the silicon carbide compound $Si_{1-x}C_x$ comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide.

3.(Amended) The [transistor] system of claim 1[, wherein the gate comprises microcrystalline silicon carbide.] wherein:

the semiconductor surface layer comprises p-type silicon;

the gate is separated from the channel region by gate oxide or tunnel oxide;

the source region comprises n-type silicon; and

the drain region comprises n-type silicon.

4.(Amended) The [transistor] system of claim 1[, wherein the transistor is a p-channel device.] wherein:

the semiconductor surface layer comprises n-type silicon;

the gate is separated from the channel region by gate oxide or tunnel oxide;

the source region comprises p-type silicon; and

the drain region comprises p-type silicon.

5.(Amended) The [transistor] system of claim 1[, wherein the transistor is an n-channel device] wherein the silicon carbide compound $Si_{1-x}C_x$ is p+ doped with boron or n+ doped with phosphorus.

8.(Amended) The [transistor] system of claim 1[, wherein the gate is separated from the channel by an insulating layer.] wherein:

the addressing circuitry further comprises:

a row decoder; and

a column decoder;

the memory device further comprises a voltage control switch; and

the system further comprises control lines, address lines, and data lines coupled between the processor and the memory device.

9.(Amended) The [transistor] system of claim [8,] 1 wherein the gate is separated from the channel region by an insulating layer that is approximately between 50 angstroms and 100 angstroms thick.

10.(Amended) The [transistor] system of claim [8,] 9 wherein the insulating layer is approximately 100 angstroms thick.

37.(Twice Amended) A [transistor] memory device comprising:

an array of memory cells comprising a plurality of transistors, at least one of the transistors comprising:

a substrate having a source region, a drain region, and a channel region between the source region and the drain region formed in the substrate;

an insulating layer on the substrate over the channel region; and

a gate comprising a p+ doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer, wherein x is less than 0.5, the gate being electrically interconnected to receive an input signal.

38.(Twice Amended) The [transistor] memory device of claim 37 wherein:

the substrate comprises a silicon surface layer formed on an underlying insulating portion having a source region, a drain region, and a channel region between the source region and the drain region formed in the silicon surface layer;

the insulating layer comprises gate oxide or tunnel oxide;

the silicon carbide compound $Si_{1-x}C_x$ comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide; [and]

the silicon carbide compound $Si_{1-x}C_x$ is p+ doped with boron[.]; and

further comprising:

a row decoder coupled to the array;

a column decoder coupled to the array;

a voltage control switch; and

control circuitry coupled to the array to control read, write, and erase operations of the memory device.

39.(Amended) The [transistor] memory device of claim 37 wherein:

the substrate comprises p-type silicon;

the source region comprises n-type silicon; and

the drain region comprises n-type silicon.

40.(Amended) The [transistor] memory device of claim 37 wherein:

the substrate comprises n-type silicon;

the source region comprises p-type silicon; and

the drain region comprises p-type silicon.

41.(Twice Amended) A [transistor] memory device comprising:

an array of memory cells comprising a plurality of transistors, at least one of the transistors comprising:

a substrate having a source region, a drain region, and a channel region between the source region and the drain region formed in the substrate;

an insulating layer on the substrate over the channel region; and

a gate comprising an n+ doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer, wherein x is less than 0.5, the gate being electrically interconnected to receive an input signal.

42.(Twice Amended) The [transistor] memory device of claim 41 wherein:

the substrate comprises a silicon surface layer formed on an underlying insulating portion

having a source region, a drain region, and a channel region between the source region and the drain region formed in the silicon surface layer;

the insulating layer comprises gate oxide or tunnel oxide;

the silicon carbide compound $Si_{1-x}C_x$ comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide; [and]

the silicon carbide compound $Si_{1-x}C_x$ is n+ doped with phosphorus[.]; and

further comprising:

a row decoder coupled to the array;

a column decoder coupled to the array;

a voltage control switch; and

control circuitry coupled to the array to control read, write, and erase operations of the memory device.

43.(Amended) The [transistor] memory device of claim 41 wherein:

the substrate comprises p-type silicon;

the source region comprises n-type silicon; and

the drain region comprises n-type silicon.

44.(Amended) The [transistor] memory device of claim 41 wherein:

the substrate comprises n-type silicon;

the source region comprises p-type silicon; and

the drain region comprises p-type silicon.

45.(Twice Amended) A [transistor] memory device comprising:

an array of memory cells comprising a plurality of transistors, at least one of the transistors comprising:

[a semiconductor surface layer formed on an underlying insulating portion having] a source region, a drain region, and a channel region between the source region and the

drain region formed in [the] a semiconductor [surface layer] substrate;

an insulating layer on the semiconductor [surface layer] substrate over the channel region; and

a gate comprising a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is less than 0.5, the gate being electrically interconnected to receive an input signal.

46.(Amended) The [transistor] memory device of claim 45 wherein:

the semiconductor [surface layer] substrate comprises a p-type silicon surface layer formed on an underlying insulating portion;

the insulating layer comprises gate oxide or tunnel oxide;

the silicon carbide compound $Si_{1-x}C_x$ comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide;

the source region comprises n-type silicon; and

the drain region comprises n-type silicon.

47.(Amended) The [transistor] memory device of claim 45 wherein:

the semiconductor [surface layer] substrate comprises an n-type silicon surface layer formed on an underlying insulating portion;

the silicon carbide compound $Si_{1-x}C_x$ comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide;

the insulating layer comprises gate oxide or tunnel oxide;

the source region comprises p-type silicon; and

the drain region comprises p-type silicon.

48.(Twice Amended) The [transistor] memory device of claim 45 wherein the silicon carbide compound $Si_{1-x}C_x$ is p+ doped with boron or n+ doped with phosphorus.

50.(Twice Amended) A [transistor] system comprising:

a processor; and

a memory device coupled to the processor, the memory device comprising:

an array of memory cells comprising a plurality of transistors, at least one of the transistors comprising:

[a semiconductor surface layer formed on an underlying insulating portion having] a source region, a drain region, and a channel region between the source region and the drain region formed in [the] a semiconductor [surface layer] substrate;

an insulating layer on the semiconductor [surface layer] substrate over the channel region; and

a gate comprising a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is less than 0.5, the gate being electrically interconnected to receive an input signal.

51.(Twice Amended) The [transistor] system of claim 50 wherein:

the semiconductor [surface layer] substrate comprises a p-type silicon surface layer formed on an underlying insulating portion;

the insulating layer comprises gate oxide or tunnel oxide;

the silicon carbide compound $Si_{1-x}C_x$ comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide;

the source region comprises n-type silicon; and

the drain region comprises n-type silicon.

52.(Amended) The [transistor] system of claim 50 wherein:

the semiconductor [surface layer] substrate comprises an n-type silicon surface layer formed on an underlying insulating portion;

the silicon carbide compound $Si_{1-x}C_x$ comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide;

the insulating layer comprises gate oxide or tunnel oxide;

the source region comprises p-type silicon; and

the drain region comprises p-type silicon.

53.(Twice Amended) The [transistor] system of claim 50 wherein the silicon carbide compound $Si_{1-x}C_x$ is p+ doped with boron or n+ doped with phosphorus.

55.[New] The memory device of claim 45, further comprising:

a row decoder coupled to the array;

a column decoder coupled to the array;

a voltage control switch; and

control circuitry coupled to the array to control read, write, and erase operations of the memory device.

56.[New] The system of claim 50 wherein:

the memory device further comprises:

a row decoder coupled to the array;

a column decoder coupled to the array;

a voltage control switch; and

control circuitry coupled to the array to control read, write, and erase operations of the memory device; and

the system further comprises control lines, address lines, and data lines coupled between the processor and the memory device.

57.[New] A system comprising:

a processor; and

a memory device coupled to the processor through control lines, address lines, and data lines, the memory device comprising:

an array of memory cells comprising a plurality of transistors, each of the transistors comprising:

a source region, a drain region, and a channel region between the source region and the drain region formed in a semiconductor substrate;

an insulating layer on the semiconductor substrate over the channel region;